REMARKS

Applicant respectfully traverses and requests reconsideration.

Applicant respectfully notes a discrepancy in the Office Action Summary. Line item 5 states that Claim 12 is allowed, while line item 6 states that Claim 12 is rejected. In accordance with the Page 2, ¶2 and Page 5, ¶8 of the Office Action, Applicant interprets the Office Action Summary to read that Claim 12 is allowable. Applicant wishes to thank the Examiner for notice that Claims 1, 6, 12 and 17 are allowable.

An informality has been corrected on page 8 of the Specification. Specifically, the step in which a determination is made as to whether the data is cached has been relabeled to correspond to step 60 as illustrated in Applicant's FIG. 5.

Claims 7 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nakatsuka et. al., U.S. 6,433,782 ("Nakatsuka") and Pedneau, U.S. 6,304,944 ("Pedneau"). In general, Claim 7 corresponds to steps 70-78 of Applicant's FIG. 6. After translating a virtual address into an address as required by step 70 of FIG. 6, the process proceeds to step 72 where a determination is made as to whether the address corresponds to a translation memory space. The Specification teaches that one such translation memory space may be the AGP window, but could be any address that is further translated from the physical memory address. (Page 8, Lines 20-22.) When the address does not correspond to the translation memory space, the translated address is cached in a translation look-aside table ("TLB"). However, when the address does correspond to another translation memory space, the address is further translated into another address and later cached in the TLB. With such a method, a single TLB within the CPU can be utilized to perform both the fist translation of a virtual address into an address (FIG. 6, Step 70) and the second translation of the address into another address (FIG. 6, Step 76). The

Specification teaches that this method reduces the complexity, redundancy and extra processing required in prior art systems. (Page 5, Line 29 - Page 6, Line 3; Page 9, Lines 6-13).

Applicant respectfully repeats the relevant remarks made in the response submitted on 1/29/03 corresponding to the Examiner's first Office Action (mailed on 08/29/02). Specifically, Applicant respectfully notes that the Nakatsuka reference appears to teach a conventional approach to address translation and simply states in the Examiner's cited section (Col. 8, Line 66 - Col. 9, Line 40) that a logical address is converted into a physical address when the data belongs in a particular program region.

As illustrated in by FIG. 1 of Nakatsuka, there are two distinct memory regions within a data process apparatus, a program region and a graphic region. During processing, data must be accessed from memory, and the region determining unit of the data processing apparatus determines to which region of the memory unit accessed data belongs. The address assignments corresponding to the two memory regions and the corresponding physical address are illustrated in Nakatsuka's FIGs. 3b-3c. FIG. 3d shows the relationship among the physical addresses of the memory unit, the logical addresses of the data processor and the picture logical addresses of the graphic processor. It is apparent that the physical addresses directly correspond to the picture logical addresses of the graphic processor while there is no such relationship between the physical addresses and the logical addresses of the data processor.

If it is determined by the region determining unit that the data belongs to the graphic region, then access between the physical address and the picture logical address of the graphic process can be achieved *without address translation.* (Emphasis Added). In contrast, when the region determining unit determines that accessed data belongs to the data region, a conventional approach to address translation is required.

Because of the foregoing, Nakatsuka merely teaches the process in which an address is translated if a region determining unit determines that the corresponding data belongs in a particular region. Nakatsuka fails to teach or suggest a process in which a virtual address is first translated into an address and then a determination is made as to whether the address corresponds to a translation memory space. As taught by Applicant's Specification, a translation memory space may be the AGP window. When the address does not correspond to the translation memory space, it is directly cached in a TLB. However, when the address corresponds to the translation memory space as claimed, it is further translated into another address prior to caching the other address in the TLB. Hence, at least two translations are required by Applicant's claimed invention when the address corresponds to translation memory space. This two-level translation based on whether translation memory space is desired is not disclosed in the cited section of the reference.

Pedneau is directed at a mechanism for storing system level attributes and translation lookaside buffer. The method and apparatus improves the efficiency of the cacheability determination by making the information for the region register available *during* linear to physical address translation, rather than *serially* upon completion of the address translation as depicted in Pedmu's FIG. 1. (*See Abstract;* Emphasis Added). The Examiner's citation to Pedneau (Col. 1, Lines 30-56; Col. 2, Lines 34-40) is in reference to an established method in which a logical address is translated into a linear address by a segmentation unit in a processor's memory management unit (MMU). (Column 1, lines 40-50). *When a paging technique is enabled*, the paging mechanism further translates the linear address into a physical address which can be used to access a requested memory location. (Emphasis Added). Prior to being used for

accessing the memory, however, the physical address is compared to the cacheability ranges stored in a regions register. (Column 1, lines 50-60).

In contrast to Applicant's claimed invention, Pedneau first describes a method in which a logical address is translated into a linear address via a segmentation unit without the use of a TLB. (FIGs. 2-4. 10). Similar to Nakatsuka, Pedneau merely discloses, inter alia, the method in which a linear address is translated into a physical address. Pedneau fails to teach or suggest elements b-e of Applicant's Claim 7. Specifically, Pedneau is silent as to a method for virtual address translation comprising the step of translating an address that has already undergone a first translation (Claim 7a) into another address *when the address corresponds to translation memory space.* (Claim 7d; Emphasis Added). The Specification teaches that a translation memory space is addressing that requires further translation from the physical memory address and may include the AGP window. (Page 8, Lines 19-24). While Applicant's claimed invention allows two translations of an address, Pedneau merely teaches the process in which one translation can take effect on a linear address. In contrast, Pedneau is primarily directed at improving the efficiency of the cacheability and other system-level attributes during linear to physical translation (when paging is enabled).

Moreover, because Pedneau does not appear to teach a second translation, Pedneau also fails to teach the method in which the translated addresses are cached in the same TLB as claimed by Applicant (Claim 7c and 7e). As a direct consequence there is no motivation to combine the two cited references because neither reference, individually or in combination, benefits from a "CPU that can perform both physical address translations and physical address translations into the AGP window space without the need for the north bridge." "A single TLB

may instead be utilized to perform such address translations" reducing the complexities of the prior art. (Page 9, Lines 6-10).

Because, no combination of Nakatsuka or Pedneau teaches or suggests Applicant's Claim 7, Claim 7 is believed to be allowable over the cited references. Claim 18 corresponds to the module claim of Claim 7 and is also believed to be in proper form for allowance.

Claims 8-11 and 19-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nakatsuka and Pedneau and further in view of Hays et al., US 6,356,989 ("Hayes"). Applicant respectfully repeats the relevant remarks made above with respect to Claims 7 and 18. Furthermore, Claims 8-11 and 19-22 contain additional novel and non-obvious subject matter and are believed to be in proper condition for allowance.

Applicant respectfully submits that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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